CLAIMS

What is claimed is:

1. A processor comprising:

a first logic (310) to convert a first operand (306, 308) from a first format (502, 520, 530) into a second format (602, 630, 650); and

a second logic (352, 354) to combine a portion of the converted first operand with a portion of a second operand that is in the second format.

2. The processor of claim 1, further comprising a third logic (318) to compare a first exponent corresponding to the first operand with a second exponent of the second operand.

3. The processor of claim 1, wherein the second logic combines a plurality of single precision operands in a same path (304) as a double precision exponent or a double-extended precision path.

4. The processor of claim 1, further comprising a third logic (310) to convert the second operand from a third format into the second format.

5. The processor of claim 1, wherein the second logic combines the portion of the converted first operand and the portion of the second operand by an addition operation or a subtraction operation.

6. The processor of claim 1, further comprising a third logic (397) to round results of the combination by the second logic.

7. The processor of claim 1, further comprising a third logic (344) to analyze a portion of the converted first operand and the second operand to determine whether one of the first or second operands corresponds to a denormal operand.

accordance with a comparison (318) of a first exponent corresponding to the first operand and a second exponent corresponding to the second operand.

16. The system of claim 15, further comprising a fourth logic (352, 354) to combine a portion of the first operand and a portion of the second operand.

17. The system of claim 15, further comprising a fourth logic (344) to analyze a portion of the first operand and the second operand to determine whether one of the first or second operands corresponds to a denormal operand.

18. The system of claim 15, wherein the memory comprises one or more of a level 1 cache, a mid-level cache, or a last level cache.

19. The system of claim 15, further comprising a plurality of processor cores (106) to access the data stored in the memory.

20. The system of claim 15, further comprising an audio device (947).

8. The processor of claim 1, further comprising one or more processor cores (106), wherein at least some of the one or more processor cores comprise one or more of the first logic or the second logic.

9. The apparatus of claim 8, wherein at least one of the one or more processor cores (106), the first logic, and the second logic are on a same die.

10. A method comprising:

modifying (704) a plurality of operands into a same format; and

combining (710) a plurality of mantissas corresponding to the modified plurality of operands.

11. The method of claim 10, further comprising comparing (706) portions of the modified plurality of operands.

12. The method of claim 10, further comprising aligning (708) portions of the plurality of mantissas.

13. The method of claim 10, further comprising normalizing (712) results of the combination of the plurality of mantissas.

14. The method of claim 10, further comprising rounding (714) results of the combination of the plurality of mantissas.

15. A system comprising:

a memory (108, 114, 116) to store data;

a first logic (202) to fetch an opcode (312), a first operand (306), and a second operand (308) from the memory;

a second logic (310) to modify the first operand and the second operand into a same format; and

a third logic (324, 326) to align one of the first or second operands in